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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/521,586	Applicant(s) ROOS ET AL.	
	Examiner Keith Vicary	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _03 September 2008_.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-20_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-20_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are pending in this application and presented for examination. Claims 1, 8, 12, 15, and 17 are newly amended by amendment filed 9/3/2008.

Claim Objections

2. Claim 1 is objected to because of the following informalities. Appropriate correction is required.

a. Claim 1 recites the limitation “in the directionally transfer of data packets” in the last 2 lines, which should presumably be “in the directional transfer of data packets".

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-7 and 15 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

5. Claim 1 recites the limitation “reducing risks of delays in the directionally transfer of data packets through the pipeline” in the last two lines. However, the original disclosure does not appear to disclose this limitation.

b. Claims 2-7 and 15 are rejected for failing to alleviate the rejection of claim 1 above.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 17-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Claim 17 recites the limitation "the at least one external device" in lines 6-7. There is insufficient antecedent basis for this limitation in the claim.

c. Claims 18-20 are rejected for failing to alleviate the rejection of claim 17 above.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1-16 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cataldo (Net processor startup takes pipelined path to 40 Gbits/s) in view of Dorst (20040098549 A1) in view of Harriman (US 6330645 B1).

11. Consider claims 1 and 8, Cataldo discloses a programmable pipeline adapted to directionally transfer data packets through the pipeline from a first end of the pipeline to a second end of the pipeline, and adapted to perform sequences of instructions on the data packets, the pipeline comprising plural pipeline stages being arranged in a row between the first end of the pipeline and the second end of the pipeline (Page 1, second to fifth paragraphs, programmable pipeline architecture…PISC can be programmed to do tasks…each PISC stage acts as a mini-processor).

However, Cataldo does not disclose the pipeline comprises plural access points being arranged in a row between the first end of the pipeline and the second end of the pipeline, the access points providing at least one external device with access to the pipeline, at least one of the access points separating and connecting two of the pipeline stages, and does not disclose at least one interface engine adapted to be connected to at least one external device located externally of the processor; the at least one interface engine is connected to the plural access points, and wherein the at least one interface engine is adapted to receive a request from any one of the connected access points of the programmable pipeline, the request being received upon arrival of one of the data packets at the respective any one access point, ii) to send a request output to the external device, the request output being based at least partly on the request from the one access point, iii) responsive to the request output, to receive an external reply

from the external device, and iv) to send to the pipeline a response, based on the external reply, to the request. Cataldo also does not disclose that the interface engine includes an arbiter configured to allow forwarding of requests from the connected access points in a fair manner between each of the connected access points, and with respect to claim 1, reducing risks of delays in the directionally transfer of data packets through the pipeline.

On the other hand, Dorst does disclose at least one interface engine (figure 3, memory controller 1005, which includes interface circuitry 4010 as shown in figure 4) adapted to be connected to at least one external device located externally of the processor (figure 3 shows multiple memories 1015 external to the processor and connected to the data processing block 3005, which includes the memory controller); the at least one interface engine is connected to plural access points, ([0031], several processors may share a memory controller; each processor is an access point or contains an access point), and wherein the at least one interface engine is adapted to i) receive a request from any one of the connected access points ([0010], memory controller couples to the processors and to the memories, and provides communication between the processor and memories; it is inherent that this communication includes a request for data in a memory by the processor), ii) to send a request output to the external device, the request output based at least partly on the request from the one access point (figure 6, control signals, explained further in [0045] and [0046]; it is inherent that which of the external devices gets the control signals is based upon the data address or other parameter in the memory access instruction), iii) responsive to the

request output, to receive an external reply from the external device ([0040], memory retrieves the data and makes it available through data bus 4020; the newly retrieved data is the external reply), and iv) to send to the access point a response, based on the external reply, to the request (Figure 1, given the memory controller connects the processor and memories together, it is inherent that the retrieved data would be passed on to the pipeline).

The teaching of Dorst reduces the burden and overhead of processors interfacing with and controlling the memory (Dorst, [0003]), as well as flexibly controls a multitude of memory circuits in a simple-to-use manner (Dorst, [0006]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Dorst with the invention of Cataldo in order to reduce the burden and overhead of processors interfacing with and controlling the memory, as well as flexibly control a multitude of memory circuits in a simple-to-use manner. Note that the teaching of Dorst, when applied to the invention of Cataldo, teach the overall limitation that the pipeline comprises plural access points being arranged in a row between the first end of the pipeline and the second end of the pipeline, the access points providing at least one external device with access to the pipeline, at least one of the access points separating and connecting two of the pipeline stages (a PISC stage of Cataldo which connects to the memory controller of Dorst would be the access point, and this PISC stage would be arranged between the first end of the pipeline and the second end of the pipeline, provide data from a memory to the pipeline, and itself be between two other PISC stages).

Dorst discloses in [0031] that several processors may share a memory controller as persons of ordinary skill in the art would understand; however, both Cataldo and Dorst also do not explicitly disclose that the interface engine includes an arbiter configured to allow forwarding of requests from the plural access points in a fair manner between each of the plural access points.

Although the examiner believes it would have been readily recognized to one of ordinary skill in the art at the time of the invention that there must be some form of arbitration given that multiple processors are sharing a memory controller which cannot handle all their requests at one time, Harriman nevertheless discloses of an arbiter configured to allow forwarding of requests from plural access points in a fair manner between each of the plural access points (col. 4, lines 19-40, arbiter 224, round robin scheme).

Harriman's teaching allows for forwarding of requests from plural access points to be done in a fair manner (Harriman, as cited above, col. 4, lines 19-40) to provide equal access to different requesters (Harriman, col. 4, lines 29-32).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Harriman with the invention of Cataldo and Dorst in order to provide equal access to different requesters. With regard to claim 1, note that the combination of Harriman into the invention of Cataldo and Dorst teaches the overall limitation of the arbiter reducing risks of delays in the directionally transfer of data packets through the pipeline (Cataldo as cited above teaches of the directional transfer of data packets through the pipeline, Harriman’s teaching of equal access to

different requestors thus reduces risks of delays for a requestor in that a single requestor cannot be starved).

12. Consider claims 2 and 9, Dorst discloses the request comprises a first request code according to a first coding scheme (it is inherent that a data instruction such as a load or store has parameter bits to indicate the address or memory module that needs to be accessed; these bits correlate to the request code and its format to be recognized is the coding scheme), the interface engine being adapted to execute a program ([0070] and [0071] discloses using finite state machines, counters, and programmable registers in order to implement the control circuitry for the memory controller and establish relative timing relationships among control signals and address signals, which is in effect executing a program), the execution being dependent upon the first request code ([0071] discloses that programmable registers provide a mechanism for timing among control signals, and [0039] specifically discloses that the programmable registers store read timing-parameters and write timing-parameters. Because [0042] discloses that each memory may correspond to a respective register set, it is inherent that, once a memory instruction occurs and its relevant parameters are sent to the memory controller, the bits regarding the specific address or memory to be accessed are used in some form to select the register with the timing-parameters relevant to that specific address or memory. These timing-parameters are used by the finite state machine to execute the program, as certain control signals are asserted at certain times to certain memory because of the parameters/code of the memory instruction), and to obtain, as a

result of the execution of the program, at least one device control code, according to a second coding scheme (succinctly stated in the third sentence of the abstract, the interface circuitry communicates with the memory by providing a plurality of control signals; as explained above, certain control signals, correlating to device control code, are asserted at certain times as a result of executing the finite state machine that correlates to the memory bring accessed. This second coding scheme is the code that is outputted to the memory which controls the memory, as opposed to the first coding scheme which is the code that makes up the instruction), in addition to which the interface engine is adapted to send the device control code to the external device, or the request output is based at least partly on the device control code ([0045], the memory controllers control a wide variety of memories with the control signals described in [0046]).

13. Consider claims 3 and 10, Dorst discloses the device control code is an operational code of the external device ([0046], the control signals serve to operate the external device).

14. Consider claims 4 and 11, Dorst discloses the program is stored in a microcode memory included in the interface engine ([0070], finite state machine; it is inherent that the finite state machine contains a register to store state variables, and the state variables determine which control signals (in essence, microinstructions that control an overall memory machine instruction) are outputted given that state).

15. Consider claims 5 and 12, Dorst discloses the pipeline comprises a plurality of access points ([0031], several processors may share a memory controller; each processor is an access point), and the interface engine is adapted to receive a request from at least one of the access points ([0031], several processors may share a memory controller; each processor is an access point), the interface engine comprising a reply control unit (figure 3, memory controller 1005 still) adapted to receive at least one receiver ID signal related to the request, and to determine, based on the receiver ID signal, the access point which is to receive the response (it is inherent that given a plurality of processors sharing the same memory controller, a processor which requests data from memory for itself would be the one to actually receive data. Because of this, it is further inherent that there must be an ID signal, either explicitly given by the processor identifying itself or implicit in that merely sending a memory instruction to the memory controller is an implicit signal as the memory controller is capable of identifying which processor sent that memory instruction, perhaps due to the pins at which it was received on).

16. Consider claims 6 and 13, Dorst discloses the reply control unit is adapted to receive an input control signal ([0010], memory controller couples to the processor and to the memories, and provides communication between the processor and memories; it is inherent that this communication includes a request for data in a memory by the processor; this request for data correlates to the input control signal, as the request for

data is inputted into the memory controller in order to control the memory into outputting the data), based on which timing information for receiving the external reply from the external device can be determined ([0071] discloses that programmable registers provide a mechanism for timing among control signals, and [0039] specifically discloses that the programmable registers store read timing-parameters and write timing-parameters. Because [0042] discloses that each memory may correspond to a respective register set, it is inherent that, once a memory instruction occurs and its relevant parameters are sent to the memory controller, the bits regarding the specific address or memory to be accessed are used in some form to select the register with the timing-parameters relevant to that specific address or memory. These timing-parameters are used by the finite state machine to execute the program, as certain control signals are asserted at certain times to certain memory because of the parameters/code of the memory instruction. One of these control signals, as seen in Table 1 near [0053], is read-enable pulse-width, which is used to program the number of cycles the read-enable signal remains asserted during read operations).

17. Consider claims 7 and 14, Dorst discloses the pipeline comprises a plurality of access points ([0031], several processors may share a memory controller; each processor is an access point), whereby the number of access points adapted to send a request to the interface engine can be adjusted ([0031], which first discloses that a system may have more than one processor and more than one memory controller. It then discloses that several processors *may* share a memory controller. If several

processors *may* share a memory controller, then it is possible that several processors *do not* share a memory controller; and if a given processor is not able to access all memory controllers, then it is apparent that they cannot send a request to that memory controller either. Furthermore, because it is disclosed that several processors *may* share a memory controller, or vice-versa, it is inherent that which is actually the case is adjustable).

18. Consider claims 15, 16, and 20, Harriman discloses the fair manner of the arbiter is a round-robin manner between the plurality of access points (col. 4, lines 19-40, arbiter 224, round robin scheme).

19. Consider claim 19, although Dorst discloses in [0031] that several processors may share a memory controller as persons of ordinary skill in the art would understand; however, both Cataldo and Dorst also do not explicitly disclose that the interface engine includes an arbiter configured to allow forwarding of requests from the plurality of access points in a fair manner between each of the plurality of access points.

Although the examiner believes it would have been readily recognized to one of ordinary skill in the art at the time of the invention that there must be some form of arbitration given that multiple processors are sharing a memory controller which cannot handle all their requests at one time, Harriman nevertheless discloses of an arbiter configured to allow forwarding of requests from the plurality of access points in a fair

manner between each of the plurality of access points (col. 4, lines 19-40, arbiter 224, round robin scheme).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Harriman with the invention of Cataldo and Dorst in order to provide equal access to different requesters (Harriman, col. 4, lines 29-32). It would have been readily recognized to one of ordinary skill in the art at the time of the invention that the teaching of Harriman fits into the environment of Cataldo and Dorst: like Cataldo and Dorst, the plural access points of Harriman are processing logic and the requests are memory requests.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Harriman with the invention of Cataldo and Dorst in order to provide equal access to different requesters.

20. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cataldo in view of Dorst.

21. Consider claim 17, Cataldo discloses a programmable pipeline comprised of plural pipeline stages located between a first end of the pipeline and a second end of the pipeline (Page 1, second to fifth paragraphs, programmable pipeline architecture…PISC can be programmed to do tasks…each PISC stage acts as a mini-processor; these access points are each processor or its corresponding ports), the pipeline configured to directionally transfer data packets from the first end to the second

end (Page 1, second to fifth paragraphs, programmable pipeline architecture…PISC can be programmed to do tasks…each PISC stage acts as a mini-processor).

However, Cataldo does not disclose that the pipeline comprises access points being located between a first end of the pipeline and a second end of the pipeline, the access points providing at least one external device with access to the pipeline, at least some of the access points separating and connecting an adjacent two of the pipeline stages, and does not disclose of an interface engine, having a reply control unit, connected to an external device located externally of the processor, and connected to the plurality of access points, the interface engine configured to i) receive a request from the pipeline upon arrival of a data packet at any one of the connected access points, ii) send a request output to the external device, the request output based at least partly on the request, iii) responsive to the request output, receive an external reply from the external device, and iv) send a response, based on the external reply, to the pipeline, and the reply control unit configured to i) receive a receiver ID signal related to the request, and ii) determine, based on the receiver ID signal, the any one of the plurality of access points of the pipeline to receive the response .

On the other hand, Dorst does disclose at least one interface engine (figure 3, memory controller 1005, which includes interface circuitry 4010 as shown in figure 4), having a replay control unit (figure 3, memory controller 1005 still), connected to at least one external device located externally of the processor (figure 3 shows multiple memories 1015 external to the processor and connected to the data processing block 3005, which includes the memory controller), and connected to the plurality of access

points, ([0031], several processors may share a memory controller; each processor is an access point or contains an access point), the interface engine configured to i) receive a request from one of the connected access points ([0010], memory controller couples to the processors and to the memories, and provides communication between the processor and memories; it is inherent that this communication includes a request for data in a memory by the processor), ii) send a request output to the external device, the request output based at least partly on the request (figure 6, control signals, explained further in [0045] and [0046]; it is inherent that which of the external devices gets the control signals is based upon the data address or other parameter in the memory access instruction), iii) responsive to the request output, receive an external reply from the external device ([0040], memory retrieves the data and makes it available through data bus 4020; the newly retrieved data is the external reply), and iv) send a response, based on the external reply, to the access point (Figure 1, given the memory controller connects the processor and memories together, it is inherent that the retrieved data would be passed on to the access point), and the reply control unit configured to i) receive a receiver ID signal related to the request, and ii) determine, based on the receiver ID signal, the any one of the plurality of access points of the pipeline to receive the response (it is inherent that given a plurality of processors sharing the same memory controller, a processor which requests data from memory for itself would be the one to actually receive data. Because of this, it is further inherent that there must be an ID signal, either explicitly given by the processor identifying itself or implicit in that merely sending a memory instruction to the memory controller is an

implicit signal as the memory controller is capable of identifying which processor sent that memory instruction, perhaps due to the pins at which it was received on).

The teaching of Dorst reduces the burden and overhead of processors interfacing with and controlling the memory (Dorst, [0003]), as well as flexibly controls a multitude of memory circuits in a simple-to-use manner (Dorst, [0006]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Dorst with the invention of Cataldo in order to reduce the burden and overhead of processors interfacing with and controlling the memory, as well as flexibly control a multitude of memory circuits in a simple-to-use manner. Note that the teaching of Dorst, when applied to the invention of Cataldo, teach the overall limitation that the pipeline comprises access points located between a first end of the pipeline and a second end of the pipeline, the access points providing at least one external device with access to the pipeline, at least one of the access points separating and connecting an adjacent two of the pipeline stages (a PISC stage of Cataldo which connects to the memory controller of Dorst would be the access point, and this PISC stage would be arranged between the first end of the pipeline and the second end of the pipeline, provide data from a memory to the pipeline, and itself be between two other PISC stages).

22. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cataldo and Dorst as applied to claim 17 above, and further in view of Berggreen (US 20030016685 A1).

23. Consider claim 18, neither Cataldo nor Dorst disclose a quantity of the plurality of access points from which the request is received by the interface engine from the pipeline is adjustable based on one of i) a data flow rate through the pipeline, and ii) a flow capacity of the external device.

On the other hand, Berggreen does disclose of the concept of processing packets in different manners depending on one of i) a data flow rate through the pipeline and ii) a flow capacity of the external device ([0038]-[0039], for example, a first operating mode is used when the data flow rate is low and a second operating mode is used when the data flow rate is high).

Berggreen's teaching increases flexibility by catering to a wide range of configurations and environments in part on current and historical operating conditions while reducing congestion and maintaining QoS for all message types (Berggreen, [0006]-[0007]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Berggreen with invention of Cataldo and Dorst in order to increase flexibility by catering to a wide range of configurations and environments in part on current and historical operating conditions while reducing congestion and maintaining QoS for all message types. It would have been readily recognized to one of ordinary skill in the art at the time of the invention that Bergreen's teaching of processing packets in differing ways dependent on data flow rate, when applied to the invention of Cataldo and Dorst, encompasses the possibility that a memory access needed for one mode is not needed for another. Additionally, the

second mode of Berggreen involves storing received messages in a second queue which does not happen in the first mode, which is one example of how rate would determine whether a memory access occurs from a specific access point of the programmable pipeline or not. It would have been readily recognized to one of ordinary skill in the art at the time of the invention that the environment of Berggreen regarding QoS is analogous to the invention of Cataldo which can be programmed to do traffic shaping.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Berggreen with invention of Cataldo and Dorst in order to increase flexibility by catering to a wide range of configurations and environments in part on current and historical operating conditions while reducing congestion and maintaining QoS for all message types.

Response to Arguments

24. Applicant argues on page 16 that Cataldo does not disclose pipeline stages separate and connected by access points as recited, wherein the access points provide external device with access to the pipeline. However, as explained in the rejection above, Cataldo as modified by Dorst does disclose the aforementioned limitation. It is noted for reference that the previous office action relied on Cataldo to teach only of access points in general, and not access points connected to the interface engine.

25. Applicant argues on page 18 that the access points of claim 1 are not the same as the pipeline stages of Cataldo; however, there appears to be no reason why they could not be. Applicant argues that that paragraph [0036] of Dorst does not disclose of a plurality of access points being connected to an interface engine; however, as cited in the rejection, [0031] of Dorst discloses this concept.

26. Applicant argues on page 19 that it is not obvious to connect external resources to a pipeline, because a delay at one part of the pipeline will affect the data traffic in other parts of the pipeline. However, examiner has nevertheless given a proper motivation to combine the teaching of Dorst with the invention of Cataldo. It is also noted that many processors may delay one part of a pipeline which affects other parts of a pipeline (for example, a cache miss which causes pipeline stalls), however, this does not mean that the concept of connecting external resources to a pipeline becomes untenable. Applicant argues that it is not critical in Harriman for one requester that another requester receives a reply; however, it is unclear as to what makes something "critical" as Harriman discloses of a round robin scheme for fair access. Applicant argues of a specific embodiment of Harriman wherein the priority of a slow device is lowered if the slow device is requesting a large amount of data; however, Harriman still discloses of a round robin scheme, and moreover, there appears to be nothing in the instant original disclosure which would preclude this embodiment. Applicant argues that "if an access point in a pipeline does not receive a request in time, the entire pipeline will be slowed down"; however, there appears to be nothing in the original disclosure

which states how an access point in a pipeline would necessarily receive a request in time and so forth.

Conclusion

27. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Keith Vicary whose telephone number is (571)270-1314. The examiner can normally be reached on Monday - Thursday, 6:15 a.m. - 5:45 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183

/Keith Vicary/
Examiner, Art Unit 2183